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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/712,084	11/13/2003	Nicholas James Witchey	021404.0012US1	7909

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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/712,084	WITCHEY, NICHOLAS JAMES	
	Examiner	Art Unit	
	Khanh Q. Dinh	2451	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 February 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This is in response to Amendment and Remarks filed on 2/1/2010. Claims 1-11 are presented for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hovel et al., US Pat. No.7,116,681 in view of Hiles et al. US pat no.7,333,510.

As to claim 1, Hovel discloses a communication protocol converter comprising:

(a) a first modular communication jack having: a housing defining an open cavity and a segregated interior chamber, a connector port having a plurality of electrical contacts positioned within said open cavity, at least one circuit board incorporating Ethernet to raw data conversion circuitry components for a first communication protocol disposed within said interior chamber in electrical communication with the electrical contacts of said connector port; wherein the circuitry

components are positioned on both sides of the at least one circuit board (ports connecting 62(A, B) and 72(A, B) of fig.2, see fig.2, col.8 line 10 to col.9 line 20); and iv) a memory positioned on said circuit board in electrical communication with said conversion circuitry for a first communication protocol for receiving converted data (using network controller to process data conversion, see figs.1, 2, col.6 line 13 to col.7 line 50); whereby the memory is interconnected to a bi-directional data line that allows the input and output of raw data (writing and accessing data from/to the storage (68A fig.2), see col.8 line 10 to col.9 line 20) (b) a second modular communication jack having: i) a housing defining an open cavity and a segregated interior chamber; ii) a connector port having a plurality of electrical contacts positioned within said open cavity; iii) at least one circuit board incorporating Ethernet to raw data conversion circuitry components for a second communication protocol disposed within said interior chamber in electrical communication with the electrical contacts of said connector port; a memory positioned on said circuit board in electrical communication with said conversion circuitry for said second communication protocol for receiving converted data (see fig.2, col.7 line 17 to col.8 line 58) wherein the memory is connected with the bi-directional line to receive input of raw data from the first modular communication jack; and (c) a bidirectional data interface electrically interconnecting said memory of said first communication jack with said memory of said second communication jack (processing data in/out of the storage, see col.8 lines 10-58).

Hovel does not specifically disclose a controller block in the form of a microprocessor which handles all the conversion between raw data and Ethernet, including processing of digital and analog signals, as well as all of the required code protocol translations, said microprocessor utilizing embedded software to manipulate the data signal to provide data to magnetics and the

memory for storing data utilized by a controller block and to communicate with Ethernet through Ethernet interface. However, Hiles discloses a controller block in the form of a microprocessor which handles all the conversion between raw data and Ethernet, including processing of digital and analog signals, as well as all of the required code protocol translations, said microprocessor utilizing embedded software to manipulate the data signal to provide data to magnetics and the memory for storing data utilized by a controller block (memory block 65 fig.6)and to communicate with Ethernet through Ethernet interface for storing data that utilized by a controller block (memory block 65 fig.6) (using a CPU to control routing table computations and performing protocol conversions from IPV4 to IPV6 and a memory block to control the operating system or applications using Ethernet interfaces, see fig.6, col.6 line 24 to col.7 line 58). It would have been obvious to one of the ordinary skill in the art at the time the invention was made to implement Hiles' teachings into the Hovel's converter to process data information because it would have allowed the master processor to efficiently perform routing computations, network diagnostics in a communication network (see Hiles' col.7 lines 2-23).

As to claim 2, Hovel discloses said first communication protocol is Internet protocol version 4 and said second communication protocol is Internet protocol version 6 (see col.8 lines 10-58).

As to claim 3, Hovel discloses said first communication protocol is Internet protocol version 6 and said second communication protocol is Internet protocol version 4 (see fig.1, col.8 lines 10-58).

As to claim 4, Hovel discloses said conversion circuitry components of said first and second modular communications jacks includes magnetic circuitry and controller circuitry (see col.9 line 20 to col.10 line 50).

As to claim 5, Hovel discloses said conversion circuitry components includes LED circuitry (see col.9 line 20 to col.10 line 50).

As to claim 6, Hovel discloses said circuit boards each define first and second opposed sides and said conversion circuitry components are positioned on both first and second sides of said circuit boards (see col.7 line 8 to col.8 line 59 col.9 line 20 to col.10 line 50).

As to claim 7, Hovel discloses a communication protocol converter comprising:
a housing defining first and second open cavities and a segregated interior chamber; each of said open cavities incorporating a plurality of electrical contacts positioned within said open cavities to form first and second connector ports wherein said first connector port is adapted to interface with a first communication protocol and said second connector port is adapted to interface with a second communication protocol (using network controller to process data conversion, see figs.1, 2, col.6 line 13 to col.7 line 50); and at least one circuit board incorporating communication protocol conversion circuitry components disposed within said interior chamber in electrical communication with the electrical contacts of said first and second connector ports wherein said conversion circuitry bi-directionally translates communication protocols (network protocol translation, see fig.2, col.7 line 17 to col.8 line 58), wherein the housing allows for the at least

one circuit board to electronically communicate with both the first connector port and the second connector port and a microprocessor employing embedded software that converts Ethernet data from internet protocol version 4 to internet protocol version 6 (converting data from IPV4 to IPV6, see fig.2, col.7 line 17 to col.8 line 58).

Hovel does not specifically disclose a microprocessor to receive Intemet protocol 4 Ethernet data, removes the Internet protocol 4 header data, inserts Internet protocol 6 header data, recalculates the necessary Internet protocol header fields and outputs corresponding Internet protocol 6 Ethernet data and a embedded software located on flash memory which is utilized by the microprocessor to perform its functions. However, Hiles discloses a microprocessor receive Intemet protocol 4 Ethernet data, removes the Internet protocol 4 header data, inserts Internet protocol 6 header data, recalculates the necessary Internet protocol header fields and outputs corresponding Internet protocol 6 Ethernet data and a embedded software located on flash memory which is utilized by the microprocessor to perform its functions (memory block 65 fig.6) (using a CPU to control routing table computations and performing protocol conversions from IPV4 to IPV6 and a memory block to control the operating system or applications, see fig.6, col.6 line 24 to col.7 line 58). It would have been obvious to one of the ordinary skill in the art at the time the invention was made to implement Hiles' teachings into the Hovel's converter to process data information because it would have allowed the master processor to efficiently perform routing computations, network diagnostics in a communication network (see Hiles' col.7 lines 2-23).

receiving Intemet protocol 4 Ethernet data, removes the Internet protocol 4 header data, inserts Internet protocol 6 header data, recalculates the necessary Internet protocol header fields and outputs corresponding Internet protocol 6 Ethernet data

As to claim 8, Hovel discloses said protocol conversion circuitry comprises, a microprocessor incorporating embedded software for converting a first communication protocol received at said first connector port to a second communication protocol output to said second connector port (processing protocol translations, see fig.2, col.8 lines 10-58).

As to claim 9, Hovel discloses said microprocessor converts a second communication received at said second connector port to a first communication protocol output to said first connector port (see col.7 line 8 to col.8 line 59 col.9 line 20 to col.10 line 50).

As to claim 10, Hovel discloses said first communication protocol is Internet protocol version 4 and said second communication protocol is Internet protocol version 6 (see fig.1, col.8 lines 10-58).

As to claim 11, Hovel discloses said first communication protocol is Internet protocol version 6 and said second communication protocol is Internet protocol version 4 (see fig.1, col.8 lines 10-58).

Response to Arguments

4. Applicant's arguments filed on 2/1/2010 have been fully considered but they are not persuasive.

- Applicant asserts that the cited references do not disclose a controller block in the form of a microprocessor which handles all the conversion between raw data and Ethernet, including processing of digital and analog signals, as well as all of the required code protocol translations, said microprocessor utilizing embedded software to manipulate the data signal to provide data to magnetics and the memory for storing data utilized by a controller block (memory block 65 fig.6)and to communicate with Ethernet through Ethernet interface for storing data that utilized by a controller block.

Examiner respectfully point out that Hies discloses the Applicant's claimed invention by showing a controller block in the form of a microprocessor which handles all the conversion between raw data and Ethernet, including processing of digital and analog signals, as well as all of the required code protocol translations, said microprocessor utilizing embedded software to manipulate the data signal to provide data to magnetics and the memory for storing data utilized by a controller block (memory block 65 fig.6) and to communicate with Ethernet through Ethernet interface for storing data that utilized by a controller block (memory block 65 fig.6) (using a CPU to control routing table computations/routing computations and performing protocol conversions from IPV4 to IPV6 and a memory block to control the operating system or applications using Ethernet interfaces, see fig.6, col.6 line 24 to col.7 line 58) as rejected above.

As a result, cited prior art does disclose a communication protocol converter, as broadly claimed by the Applicants. Applicants clearly have still failed to identify specific claim limitations that would define a clearly patentable distinction over prior art.

Conclusion

5. Claims 1-11 are rejected.

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action

is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Dinh whose telephone number is (571) 272-3936. The examiner can normally be reached on Monday through Friday from 8:00 A.m. to 5:00 P.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, FOLLANSBEE JOHN, can be reached on (571) 272-3964. The fax phone number for this group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any response to this action should be mailed to:
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/Khanh Dinh/
Primary Examiner, Art Unit 2451